48. (New) A semiconductor integrated circuit structure comprising:

a semiconductor wafer substrate that includes a plurality of semiconductor integrated circuits are formed in an upper surface of said wafer substrate;

for each semiconductor integrated circuit die, a plurality of conductive bond pads formed on an upper surface of said integrated circuit die;

a glass sheet having a plurality of holes formed through from an upper surface of the glass sheet to a lower surface of the glass sheet;

for each hole formed in the glass sheet, an associated conductive solder ball bond pad structure having a first portion formed on the upper surface of the glass sheet in proximity to said hole and having a second portion that extends through the associated hole in the glass sheet and through the adhesive material to be electrically connected to the die bond pad associated with said hole; and

for each solder ball bond pad structure, a solder ball formed on the first portion of said solder ball bond pad structure to thereby provide an electrical connection between said solder ball and on associated die bond pad.--

REMARKS

Reconsideration of the above-identified patent application is requested in view of the remarks that follow.

In the November 21, 2000, Office Action in this application, the Examiner rejected claims 18-24 and 30-38 under 35 USC §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter regarded as the invention. Specifically, with respect to claim 8 and claim 32, the Examiner questioned use of the term "conductive material." With respect to claim 30 and 31, the Examiner objected to the use of the term "second conductive layer", suggesting that the correct term would have been "second layer of conductive material."

As indicated above, claims 18-24 and 30-38 have been canceled. New claims 39-48 have been added. New claims 39-48 have been drafted with the Examiner's §112 rejection of claims

The Examiner also rejected claims 18-32 (?) under 35 USC §103(a) as being unpatentable over the Kata et al. reference, in view of the Lin reference, the Tsukamoto reference and the Igarashi et al. reference. Since the Examiner's comments on the rejection apply to each of claims 18-32, applicant assumes that the §103(a) rejection was intended to be applied to claims 18-38, rather than to only claims 18-32.

Nevertheless, as stated above, applicant's claims 18-38 have been canceled in favor of new claims 39-48. For the reasons set forth below, applicant traverses the §103(a) rejection as it may be applied to new claims 39-48.

As stated in applicant's Summary of the Invention section of the application, the present invention is directed to a structure in which a glass sheet is affixed to a semiconductor wafer utilizing a layer of adhesive material disposed between the glass sheet and the semiconductor wafer. The glass sheet includes a pattern of holes that matches a pattern of bond pads formed on the semiconductor wafer. Thus, when the glass sheet is affixed to the wafer, the pattern of holes on the glass sheet aligns with the pattern of bond pads on the semiconductor wafer.

Note that the structure of the claimed invention is a semiconductor wafer, not an individual semiconductor die. The semiconductor wafer includes a matrix of individual semiconductor die, each die having an integrated circuit structure formed therein. Typically, in accordance with conventional integrated circuit fabrication techniques, the integrated circuit layout and, thus, the pattern of bond pads for each integrated circuit die, would be identical for all die formed in the semiconductor wafer.

As further stated in applicant's Summary of the Invention section of the application, in accordance with one aspect of the invention, metallized solder ball bond pads are formed on the glass sheet adjacent to each hole. In one embodiment of the invention, a metal trace is formed from each metallized solder ball bond pad on the glass sheet to the associated die bond pad on the semiconductor wafer under the adjacent hole. In accordance with a second aspect of the invention, the solder ball bond pad is formed on the glass sheet adjacent to the hole and includes a portion that extends down the sides of the adjacent hole. In this second embodiment, the hole is filled with a metal plug that electrically connects the solder ball bond pad on the glass sheet to

As further stated in the Summery of the Invention section of the application, in both the first aspect of the invention and the second aspect of the invention, a conductive solder ball is formed on each solder ball die pad on the glass sheet. Thus, an electrical conduction path is formed between each solder ball formed on the upper surface of the glass sheet and its associated die bond pad formed on the upper surface of the semiconductor wafer.

New independent claim 39 is directed to the first aspect of the invention described above. Specifically, new claim 39 defines a semiconductor integrated circuit structure that includes a semiconductor wafer substrate that includes a plurality of semiconductor integrated circuit die formed on the upper surface of the wafer. Each semiconductor integrated circuit die includes a plurality of conductive die bond pads formed on an upper surface of the die. As stated above, although not a required element of new claim 39, conventional integrated circuit processing techniques would cause the pattern of conductive die bond pads formed on each integrated circuit to be identical among all integrated circuits formed on the wafer. Referring back to claim 39, the claimed semiconductor integrated circuit structure further includes a glass sheet that has a plurality of holes formed in it. A conductive solder ball bond pad is formed on the upper surface of the glass sheet in proximity to each hole. An adhesive material disposed between the upper surface of the wafer substrate and the lower surface of the glass sheet affixes the glass sheet to the wafer such that each hole in the glass sheet is aligned with an associated die bond pad formed on the upper surface of each of the integrated circuit die formed in the wafer. A strip of conductive material is formed in electrical contact with each solder ball die bond pad and extends through the associated hole in the glass sheet, and through the adhesive material, to form an electrical connection to the die bond pad associated with that particular hole. A solder ball is formed on each solder ball bond pad, thereby providing an electrical connection between the solder ball and its associated die bond pad on the wafer.

Applicant's new independent claim 47 is directed to the second aspect of the invention. Without providing an element-by-element reconstruction of new independent claim 47, which applicant believes is clear on its face, applicant notes that the difference between the semiconductor integrate circuit structure defined by new claim 47 and the structure defined by new claim 39 lies in the fact that, in the claim 47 structure, the solder ball bond pad includes a

conductive plug is then formed in the hole in the glass sheet associated with the solder ball bond pad and to be in electrical contact with the second portion of the solder ball bond pad that extends into the hole. The conductive plug is formed to be in electrical contact with the associated die bond pad. Thus, when a solder ball is attached to that particular solder ball bond pad, an electrical connection is formed between that solder ball and the associated die bond pad on the wafer. This is in contrast to the claim 39 structure in which a conductive trace is formed between the solder ball bond pad formed on the upper surface of the glass sheet through the proximate hole in the glass sheet to connect to the associated die bond pad, thereby creating an electrical connection between the solder ball formed on the solder ball bond pad and the associated die bond pad on the wafer.

Applicant's new claim 48 is intended to cover both the first aspect of the invention and the second aspect of the invention. That is, applicant's new claim 48 recites that, for each hole formed in the glass sheet, an associated conductive solder ball bond pad structure is formed to include a first portion formed on the upper surface of the glass sheet in proximity to the hole and a second portion that extends through the associated hole in the glass sheet and through the adhesive material to be electrically connected to the die bond pad on the wafer that is associated with that hole. Applicant believes that this language encompasses both the "solder ball bond pad with conductive trace" and the "solder ball bond pad and metal plug" aspects of the invention, but is not intended to be limited only to these two disclosed embodiments of the invention.

Referring now to the §103 rejection set forth by the Examiner in his remarks in the November 21, 2000, Office Action , the Examiner first refers to the Kata et al reference as showing a wafer scale device where the wafer is connected through film 64 to bumps 70. The Examiner refers to Figs. 3 and 4 and to column 6, line 36 et seq. of kata et al. With reference to the sections of the Kata et al. reference cited by the Examiner, Kata et al teach an aluminum interconnection layer 60 formed on a wafer 10. The aluminum interconnection layer 60 is connected to a chip electrode 11 at one of its ends. The other end of the aluminum interconnection layer 60 extends toward the central portion of the chip 10a. Nickel plating 62 is formed on the aluminum interconnection layer 60. A polyimide cover coating film 64 is formed

However, the above-described Kata et al. structure does not include a glass sheet having a plurality of holes formed in it and affixed to an underlying semiconductor wafer utilizing an intervening adhesive material, as recited in each of applicant's new independent claims 39, 47 and 48.

The Eaminer then refers to the Lin reference as showing a flip chip device, as shown in Lin's Fiure 5. As discussed in the Lin et al. reference beginning at column 5, line 42, the structure shown in Lin's Fgure 5 demonstrates how conductive traces 26 are used to connect peripheral solder bumps 16 formed on integrated circuit die 12 by connecting the solder bumps 16 on the die 12 to the terminal pads of the conductive traces 26 which electrically route the solder bumps to vias 24. Underfill material 36 is used between the flip chip semiconductor die 12 and a printed circuit (PC) board 34. Solder balls formed on a reverse side of a rigid interposer 22 connect the traces 24 to the PC board 34. As described at column 5, lines 60-68, the rigid interposer 22 is required to be a multi-layer material having more than one conductive layer. That is, Figure 5 of the Lin reference, whish is cited by the Examiner in his support of the §103, combination applied to applicant's claims, discloses and interposer material 22 formed as a multi-layer material having more than one conductive layer; (details of the interposer 22 are provided at column 6 of the Lin reference, at lines 28-60). The interposer 22 has conductive vias 24 formed through it to electrically connect conductive traces formed on one side of the interposer 22 to solder balls 32 formed on the opposite side of the interposer 22.

This structure is completely unlike the structure defined by applicant's new claims 39, 47 and 48 in that applicant's invention, as recited in these claims, defines a sheet of glass that has solder ball bond pads formed on a first side of the glass sheet and solder balls formed on the bond pads, that is, on the same side of the glass sheet as the bond pads. The bond pads in the claimed invention extend through the glass sheet to provide electrical connection to an underlying semiconductor wafer to which the glass sheet is affixed utilizing an adhesive material.

The Tsukamoto reference is cited as showing a glass ceramic that will match the thermal

glass sheet and extending through proximate holes in the glass sheet, the glass sheet being affixed to an underlying semiconductor wafer utilizing an adhesive material such that the holes in the glass sheet align with bond pads formed in the semiconductor wafer such that the solder ball structures electrically interconnect the solder balls on the upper surface of the glass sheet to the associated bond pad structure on the upper surface of the wafer.

Similarly, although the Igarashi et al. reference is cited as showing the use of a polyimide to bond a die to an intermediate sheet, the structure recited in applicant's new claims 39, 47 and 48, as discussed in detail above, is neither taught nor suggested by the Igarashi et al. reference.

Thus, since none of the references cited by the Examiner individually teaches a key aspect of applicant's invention, that is, attachment of a glass sheet to an underlying semiconductor wafer using an adhesive material and extending electrical connections from a solder ball formed on an upper surface of the glass sheet to a die bond pad structure formed on the upper surface of the wafer, applicant submits that these references, considered individually or in combination, neither teach nor suggest the invention as defined by new independent claims 39, 47 and 48.

For the reason set forth above, it is submitted that all claims now present in this application are in compliance with all requirements of 35 USC §112 and patentably distinguish over the prior art. Therefore, it is requested that this application be passed to allowance.

Respectfully submitted,

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